Pulsed and Pulsed Bias Sputtering
Principles and Applications

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and
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Diffusion Barrier Stack - 5 nm -3 nm -2 nm :. . . -. . . . : . . O. 21-lm Figure 2: Schematic representing a cross-sectional view of the topography that is encountered in the processing of integrated circuits. (Not to scale) these sub-micron sized features is depicted in Fig. 2. The role of the diffusion barrier is to prevent the diffusion of metallic ions into the interlayer dielectric (lLD). Depending on the technology, in particular the choice of the ILD and the metal interconnect, the diffusion barrier may be Ti, Ta, TiN, TaN, or a multi-layered structure of these materials. The adhesion of the barrier to the dielectric, the conformality of the barrier to the feature, the physical structure of the film, and the chemical composition of the film are key issues that are determined in part by the nature of the deposition process. Likewise, after the growth of the barrier, a conducting layer (the seed layer) is needed for subsequent filling of the trench by electrochemical deposition. Again, the growth process must be able to deposit a film that is continuous along the topography of the sub-micron sized features. Other factors of concern are the purity and the texture of the seed layer, as both of these factors influence the final resistivity of the metallic interconnect. Sputter-deposited coatings are also commonly employed for their electro-optical properties. For example, an electrochromic glazing is used to control the flux of light that is transmitted through a glazed material.

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Pulsed and Pulsed Bias Sputtering: Principles and Applications By Edward V. Barnat, Toh-Ming Lu Bibliography

- Sales Rank: #4843558 in Books
- Brand: Brand: Springer
- Published on: 2003-09-30
- Original language: English
- Number of items: 1
- Dimensions: 9.21" h x .44" w x 6.14" l, .95 pounds
- Binding: Hardcover
- 157 pages

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