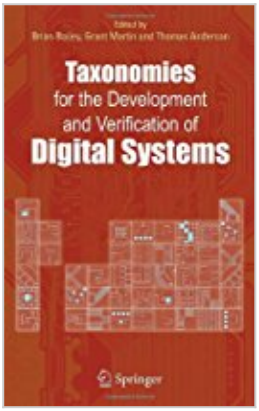

Taxonomies for the Development and Verification of Digital Systems

From Springer

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Thorough set of definitions for the terms and models used in the creation, refinement, and verification of complex systems from the conceptual level down to its implementation

Considering both the hardware and software components of the system

Also covers the emerging area of platform-based design

Provides both knowledge of models and terms, and understanding of these models and how they are used.

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Editorial Review

From the Back Cover

"In the complicated world of system-on-chip design, we need a common language so we know what we're talking about. By providing definitions for the terms used in the modeling, implementation, and verification of electronic systems, the taxonomies described in this book will help us find a common understanding." --Richard Goering, Group Editorial Director for Design Automation, Electronic Engineering Times

"Successful industries must have a firm foundation for the vaocabulary that they use to communicate ideas and to avoid misunderstandings. VSIA tackled this problem by developing a series of related taxonomies. This book includes all this material, with updates to the earlier definitions where technology has evolved. Its publication will allow greater industry penetration and ensure continued evolution over time." --Mike Kaskowitz, President, Virtual Socket Interface Alliance (VSIA)

"In the electronics world, we are often accused of not knowing what we are talking about. Unfortunately, it is all too often true. The myriad of terms and acronyms that we throw around is astounding, yet the rapid advance of technology often changes our definitions within a few years. Add to that the propensity of marketing types to hijack and redefine terms, and you have anarchy. This book is the industry's attempt to bring order to the madness. Read it and maybe we won't be fooled again." --Gary Smith, EDA Chief Analyst, Gartner Dataquest

Communication between engineers and their managers, suppliers, and customers relies on a shared vocabulary. While a common understanding of industry-specific terms is not normally a problem for those in an industry, it has proven to be a significant roadblock in the EDA field. Here, terms are created as required by any number of people, multiple terms are coined for the same thing, and even worse, the same term can sometimes be used for many different things. Though EDA-specific expressions have developed, an industry-standard terminology has not.

Without a guide to EDA vocabulary, understanding all the types of models required to design and verify modern electronics-based systems can be a major undertaking. A taxonomy solves such problems by identifying all of the significant terms used by an industry and providing a structural framework in which those terms can be defined and their relationship to other terms identified.

Taxonomies for the Development and Verification of Digital Systems provides a thorough set of definitions for the terms and models used in the creation, refinement, and verification of complex systems. The book covers systems terminology from the conceptual level to actual implementation, considers both the hardware and software components of the system, and also includes the emerging area of platform-based design. Taxonomies provide knowledge of both models and terms, as well as an understanding of how models are used.

About the Author

Brian Bailey is an independent functional verification consultant helping system designers improve their

verification efficiency, and providing guidance and technology services to small start-up companies. He has spent over 20 years creating verification solutions in a number of EDA companies and in recent years has spent most of his time helping the industry understand how and when to adopt new verification methodologies.

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Thomas Anderson is a Director of Technical Marketing at Synopsys, Inc. in Mountain View, CA and chair of the VSIA functional verification working group. Previously he was Vice President of Applications Engineering at 0-In and Vice President of Engineering at Virtual Chips. He has authored over 100 papers and technical articles on verification, IP and interface standards.

Users Review

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