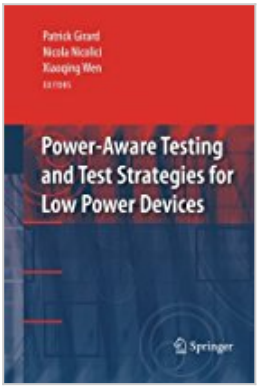

Power-Aware Testing and Test Strategies for Low Power Devices

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Managing the power consumption of circuits and systems is now considered one of the most important challenges for the semiconductor industry. Elaborate power management strategies, such as dynamic voltage scaling, clock gating or power gating techniques, are used today to control the power dissipation during functional operation. The usage of these strategies has various implications on manufacturing test, and power-aware test is therefore increasingly becoming a major consideration during design-for-test and test preparation for low power devices. This book explores existing solutions for power-aware test and design-for-test of conventional circuits and systems, and surveys test strategies and EDA solutions for testing low power devices.

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Editorial Review

From the Back Cover

Power-Aware Testing and Test Strategies for Low-Power Devices

Edited by:

Patrick Girard, Research Director, CNRS / LIRMM, France

Nicola Nicolici, Associate Professor, McMaster University, Canada

Xiaoqing Wen, Professor, Kyushu Institute of Technology, Japan

Managing the power consumption of circuits and systems is now considered as one of the most important challenges for the semiconductor industry. Elaborate power management strategies, such as voltage scaling, clock gating or power gating techniques, are used today to control the power dissipation during functional operation. The usage of these strategies has various implications on manufacturing test, and power-aware test is therefore increasingly becoming a major consideration during design-for-test and test preparation for low-power devices. This book explores existing solutions for power-aware test and design-for-test of conventional circuits and systems, and surveys test strategies and Electronic Design Automation (EDA) solutions for testing low-power devices.

1. The first comprehensive book on power-aware test for (low-power) circuits and systems
2. Shows readers how low-power devices can be tested safely without affecting yield and reliability
3. Includes necessary background information on design-for-test and low-power design
4. Covers in detail power-constrained test techniques, including power-aware automatic test pattern generation, design-for-test, built-in self-test and test compression
5. Presents state-of-the-art industrial practices and EDA solutions

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